SILICON RF GCMOS PERFORMANCE FOR PORTABLE COMMUNICATIONS APPLICATIONS

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ABSTRACT

A submicron silicon Radio Frequency Graded Channel MOS (RFGCMOS) technology has been developed for portable communications applications [1]. A 12mm device at 900 MHz has +29 dBm output power with 12 dB gain and 78% power added efficiency (PAE) at a drain to source voltage of 3.4V, and drain to source quiescent current of 150 mA. A 256 µm device at 900 MHz has 18.9 dB of small signal gain and an associated noise figure of 1.1 dB at VDS=3.0 volts and IDS=2 mA.

INTRODUCTION

This paper reports, *for the first time*, the performance of the newly fabricated RFGCMOS circuit blocks that include the receiver low noise amplifier, mixer and voltage controlled oscillator**.** The RFGCMOS technology is based on a low power, low cost GCMOS VLSI technology with the addition of fully integrated passive components and optimized GC-MOSFETs for RF operation. The technology is developed to provide a low cost, mixed-mode, and highly integrated solution for wireless applications [1]. The transmitter includes an amplifier, upconverter and voltage controlled oscillator. A 128µm wide X 0.65µm gate length device at VDS=3.0 volts and IDQ=2.0 mA exhibits Ft=11 GHz and Fmax=20 GHz.

RECEIVER ARCHITECTURE

The current sharing cascode LNA was designed to operate at 940 MHz. This two stage design provides excellent forward gain and reverse isolation. Simulation results predicted 20 dB of gain at a noise figure of 1.5 dB. The measured performance was 19 dB of gain, 39 dB reverse isolation and 1.4 dB noise figure (see Figure 1). This cascode LNA circuit is completely integrated except for two external inductors and capacitors, one each for the input and output matching networks. This cascode amplifier is followed by a saw filter centered at 940 MHz and then a cascode active mixer. The mixer topology is identical to the LNA's thus taking advantage of current sharing techniques. The first stage of the mixer functions as a common source amplifier for the RF signal that helps provide noise figure and gain performance. The LO is fed into the gate of the common gate device. Mixing is achieved by switching the common gate at the LO frequency while the RF signal is applied to the source of the common gate device, producing the 1st IF (45 MHz) at the drain. The measured performance of the mixer circuit was 9 dB conversion gain with 5.5 dB noise figure (see Figure 2).

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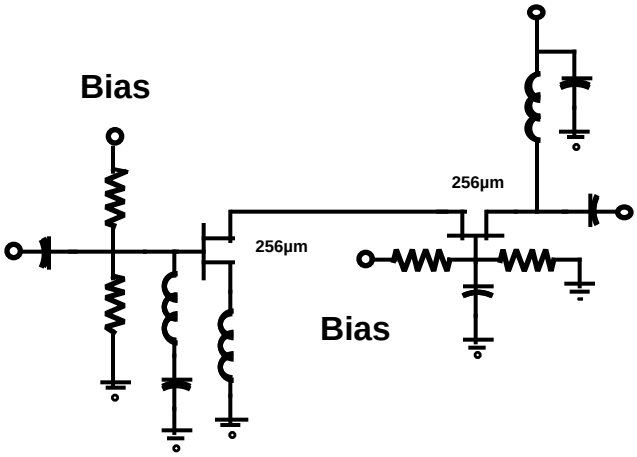


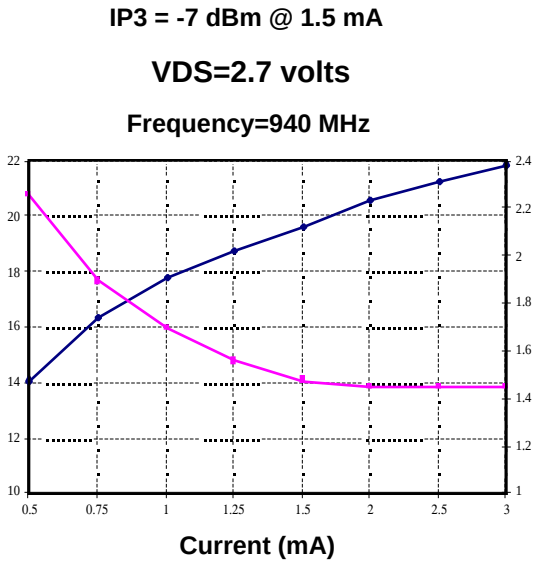


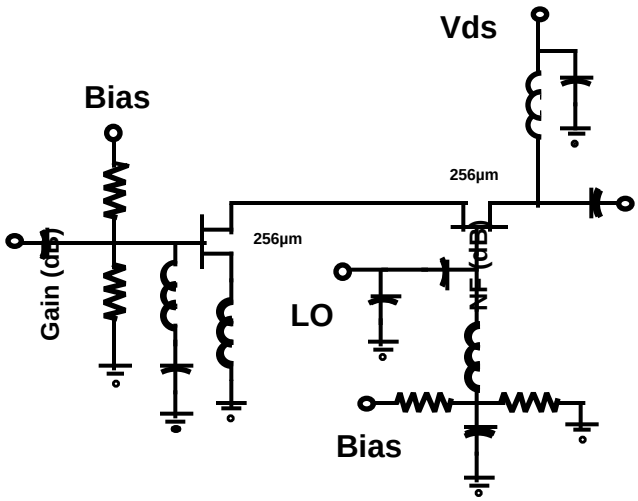
Figure 1 Cascode LNA circuit and results

The voltage controlled oscillator (VCO), shown in Figure 3, is a Colpitts topology and is completely integrated with the exception of the resonator and varactor circuitry. A negative resistance is achieved at the input of the VCO by the proper selection of feedback capacitor values, C1 and C2, according to the equations shown. This negative resistance will cancel the losses from the resonator and load to satisfy the conditions for oscillation [2].

$R=-g_m/\omega^2(C1C2)$
$Cin=C1C2/(C1+C2)$

A coaxial resonator and varactor are used, which adjust the frequency range of operation. The VCO exhibited an output power of -5.0 dBm and 125 dBc/Hz phase noise at 25 KHz away from the carrier. Equivalent phase noise performance to Bipolar technology is achieved here at a 50% reduction in drain current.

Total current consumption for the receiver function is 4.0 mA, with 24 dB of gain, 2.0 dB of noise figure and an input IP3 of -14 dBm.



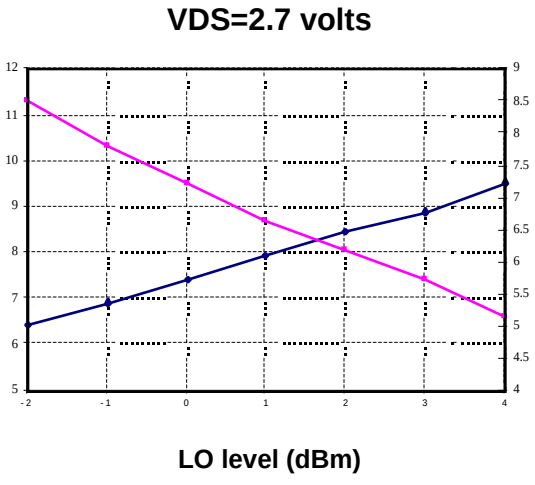


Figure 2 Cascode Mixer and Results

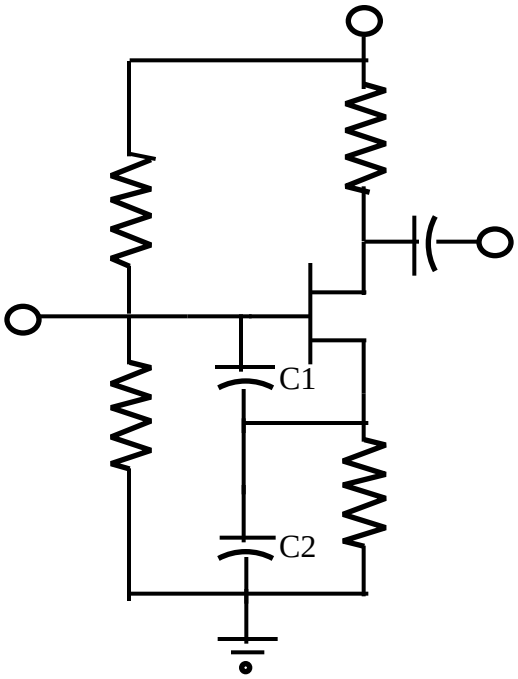


Figure 3 Integrated VCO circuit

Transmitter Architecture

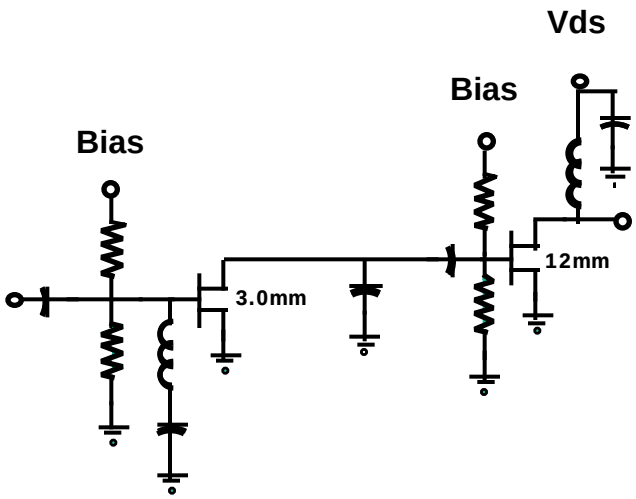
The upconverter is a Gilbert cell topology with 7.4 dB of gain at 2 mA, and an input IP3 of -10 dBm. The LO signal is mixed with the audio frequency to produce the modulated transmit carrier frequency.

The transmitter VCO is identical to the receiver VCO except for frequency range of operation (900 MHz).

The driver amplifier is a cascode topology, with over 24 dB of gain and 44 dB of isolation. The total current drain is 8 mA. *All matching components are integrated.*

The power amplifier is a 2 stage common source design with 20 dB of power gain, and an output power of +18 dBm with only 40 mA of total current drain. All matching components are on the chip with the exception of the power amplifiers output matching network. Total current drain for the transmitter is 51 mA. The transmitter is stable into a 20:1 VSWR load mismatch at all phase angles with no degradation in performance.

For higher power requirements, a 2 stage, 3.4 volt power amplifier was designed and fabricated. Simulation results predicted +30.0 dBm output power and 62% PAE. Measured results show +30.5 dBm output power and 62% PAE, small signal gain is 30 dB. At +30.5 dBm output power, the small signal gain is 25.5 dB (Fig. 4). All matching is integrated on chip except for the output matching network. This amplifier is stable into a 20:1 VSWR load mismatch with no degradation in performance.



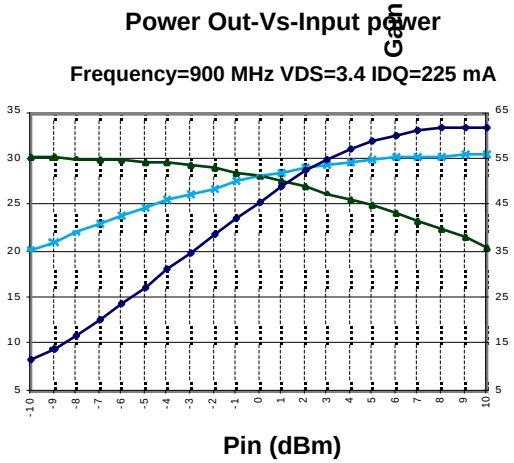


Figure 4. 2 stage Power amplifier and results

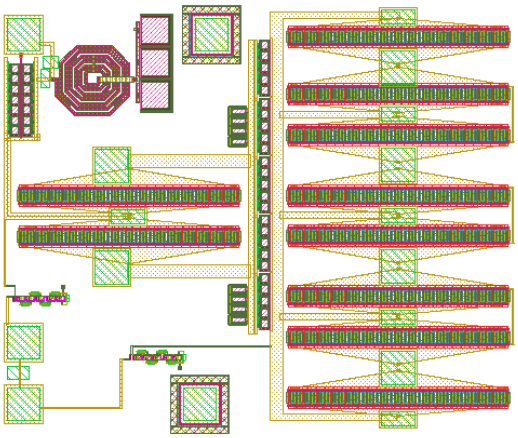


Figure 5. Layout of Power Amp

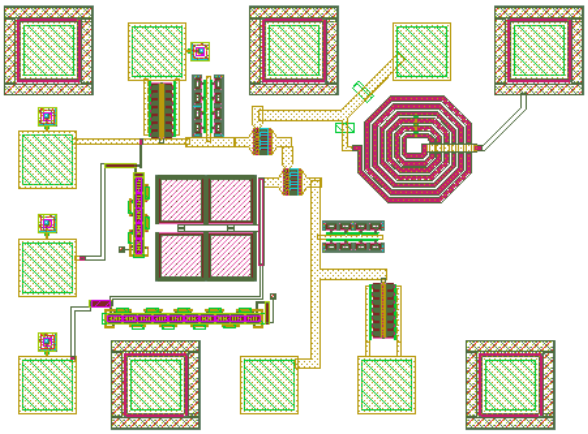


Figure 6. Layout of LNA

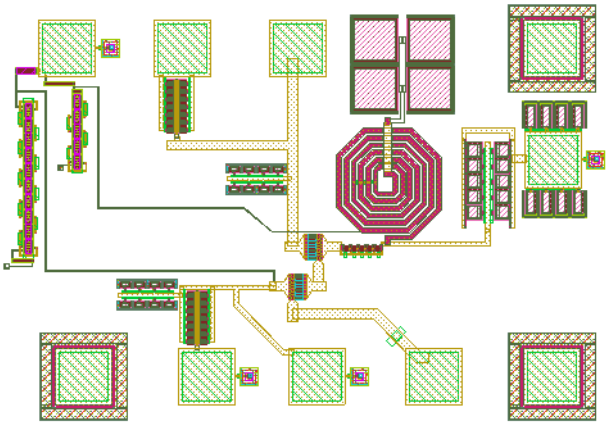


Figure 7. Layout of Mixer

Conclusion

Silicon RFGCMOS technology has been developed to provide a low cost, mixed-mode and highly integrated solution for wireless communications. The applicability of RFGCMOS for 900 MHz transceiver applications have been demonstrated by excellent RF circuit performance and low power consumption.

[1] Jun Ma, *et al.*, submitted to IEEE MTT-S 1997
[2] George Vendelin, *et al.*, Microwave Circuit Design, ISDN 0-471-60276-0